

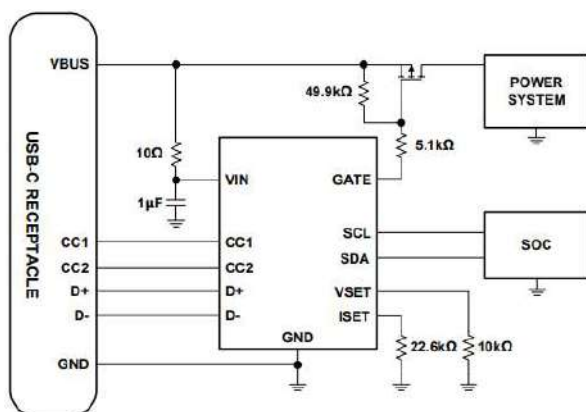
TCS8330_应用说明

ANP_TCS8330_V1.0

一、TCS8330概述

TCS8330支持PD3.0, Type-C V1.4, Apple Divider 3, BC1.2 SDP, DCP and CDP SINK通讯协议; 宽工作电压范围: 3V-25V; VBUS 耐压30V, CC脚位耐压25V; 采用DFN10_3mmX3mm 封装。

二、典型电路图及脚位说明



备注: 上图电路的PMOS可以省掉, VBUS可以和后端电路直通

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

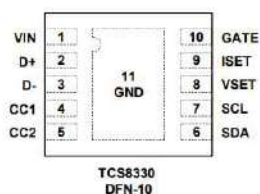


Figure 2. Pin Configuration (Top View)

Table 1. Pin Function Descriptions

Pin No.	Pin Name	Type ¹	Description
1	VIN	P	Power supply input. Connect this pin to VBUS of USB Type-C connector and bias this pin via a 1μF ceramic capacitor.
2	D+	DIO	Positive line of USB 2.0 data line for Apple Divider 3 and BC1.2.
3	D-	DIO	Negative line of USB 2.0 data line for Apple Divider 3 and BC1.2.
4	CC1	AIO	Configuration line 1 used to negotiate a voltage/current with the attached adapter.
5	CC2	AIO	Configuration line 2 used to negotiate a voltage/current with the attached adapter.
6	SDA	DIO	I ² C communication data signal.
7	SCL	DIO	I ² C communication clock signal.
8	VSET	AI	Connect a resistor to indicate the maximum voltage needed by the system from the attached power adapter.
9	ISET	AI	Connect a resistor to indicate the maximum current needed by the system from the attached power adapter.
10	GATE	OD	Open drain gate driver output. Connect this signal to the gate of an external PMOS through a series resistor. Leave this pin open if not used.
11	GND	P	Ground reference. All signals are referred to this pin.

三、选取电压与Rvset取值

R _{VSET} (kΩ)	VSET_VOLTAGE (V)
0	5
6.04	9
10	12
14	15
17.8	18
Open	20